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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,124	08/25/2003	Aurelian Vasile Lazarut	X-1391 US	3211

EXAMINER	
LEVIN, NAUM B	

ART UNIT	PAPER NUMBER
2825	

24309 7590 04/03/2006

XILINX, INC
ATTN: LEGAL DEPARTMENT
2100 LOGIC DR
SAN JOSE, CA 95124

DATE MAILED: 04/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/648,124	LAZARUT ET AL.	
	Examiner	Art Unit	
	Naum B. Levin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/648,124, and RCE filed on 01/03/2006. Claims 1-30 remain pending in the application.

2. Applicants have included additional limitations into all independent claims. The Examiner finds Applicant's comments persuasive on the application of Kittross on the claims. However, the Examiner has found another reference, which reads on the claims as presently written.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Levi et al. (US Patent 6,363,517).

4. As to claim 1, 6, 11, 16, 21 and 26 Levi discloses:

(1) A client-server semiconductor verification system, said system comprising:

a client computer storing a test job for testing a design of a programmable logic circuit (an apparatus comprises creating respective configuration bitstreams on a data processing system at a first location /the computer at the local site–col.2, ll.41-45), said test job (configuration bitstream 150, Fig. 2) having test vectors and configuration data for said programmable logic circuit (Configuration bitstream 150 includes a group of bit sequences 152 for evolving circuitry, a group of bit sequences 154 for test circuitry –

col.6, ll.10-12; the test circuitry could be configured to generate a fixed set of test vectors - col.6, ll.20-21) (col.2, ll.41-45; col.6, ll.10-24);

a server coupled to said client computer by way of a network, said server receiving said test job from said client computer (The configuration bitstreams are downloaded from the data processing system/client to a device or devices at another location, for example via a network –col.2, ll.45-48; At the remote site, a board in a computer holds an FPGA or other programmable device. This remote computer may be on the other side of the world. The two computers may communicate through a local area network, through a modem, or through the internet. A server must be provided at the remote site - col.2, ll.55-61) (col.2, ll.45-50; col.2, ll.55-65); and

a system under test coupled to said server and having said programmable logic circuit which is configured with a circuit design implemented according to said configuration data (At the remote site, a board in a computer holds an FPGA or other programmable device –col.2,ll.55-56), said system under test receiving said test vectors and outputting result vectors to the client computer by way of said server (devices at the second location then operate using bitstreams evolved at the first location, and generate results that are sent back to the first location –col.2,ll.48-50; A server must be provided at the remote site to read the incoming bitstream and configure the programmable device. The server also reads state data from the device during or after operation and feeds this data back to the computer at the local site/client – col.2, ll.60-65) (col.2, ll.45-50; col.2, ll.55-65);

(6) A client-server semiconductor verification system, said system comprising:

a plurality of client computers (The method setHardware supports the capability to evolve multiple populations of configuration bitstreams in parallel. Using the device and board identifiers and parameters, the populations can evolve on separate devices/clients. To accomplish remote internet access requires software on computer to which the remote FPGA is connected – col.11, ll.34-41), wherein a client computer of said plurality computers generates a test job for testing the design of a programmable logic circuit and comprises test vectors and configuration data for said programmable logic circuit (col.2, ll.41-45; col.6, ll.10-24; col.11, ll.34-50);

a server coupled to said plurality of client computers by way of a network, said server receiving said test job from said client computer (col.2, ll.45-50; col.2, ll.55-65); and

a system under test coupled to said server, said system under test having said programmable logic circuit which is configured with a circuit design implemented according to said configuration data and receiving said test vectors and outputting result vectors to the client computer by way of the server (col.2, ll.45-50; col.2, ll.55-65);

(11) A client- server semiconductor verification system, said system comprising:

a plurality of client computers, wherein a client computer of said plurality computers generates a test job for testing the design of a programmable logic circuit and has test vectors and configuration data for said programmable logic circuit (col.2, ll.41-45; col.6, ll.10-24; col.11, ll.34-50);

a job distribution server coupled to said plurality of client computers by way of a network, said job distribution server receiving said test job from said client computer

(The method setHardware supports the capability to evolve multiple populations of configuration bitstreams in parallel. Using the device and board identifiers and parameters, the populations can evolve on separate devices. If one device is remote from another, the transfer can be made over the internet. To accomplish remote internet access requires software on a server or computer to which the remote FPGA is connected. The XHWIF software from Xilinx, Inc. is appropriate. This software enables the remote site to receive a bitstream, which configures the FPGA, and to send a readback bitstream to the originating site for evaluating evolution of this remotely evolved bitstream - col.11, ll.34-50);

a server coupled to said plurality of client computers by way of a network, said server receiving said test job from said client computer (col.2, ll.45-50; col.2, ll.55-65); and

a system under test coupled to said server, said system under test having said programmable logic circuit which is configured with a circuit design implemented according to said configuration data and receiving said test vectors and outputting result vectors to the client computer by way of the server (col.2, ll.45-50; col.2, ll.55-65);

(16) A method of verifying semiconductor design by way of a server, said method comprising:

storing a test job for testing a design of a circuit in a client computer, said test job having test vectors and configuration data for a circuit implemented in programmable logic (col.2, ll.41-45; col.6, ll.10-24);

configuring a system under test coupled having said circuit implemented in said programmable logic to said server and having said programmable logic circuit with a circuit design according to said configuration data of said test job by way of a test server (col.2, ll.45-50; col.2, ll.55-65);

coupling said test vectors to said system under test (col.2, ll.45-47);

receiving an output comprising result vectors from said system under test (col.2, ll.48-50); and

comparing said result vectors from said system under test to expected result vectors (col.2, ll.50-54);

(21) A method of verifying a semiconductor design by way of a server, said method comprising the steps of:

coupling a plurality of client computers lo a test sever, each said client computer storing a test job for testing the design of a programmable logic circuit, said test job having test vectors and configuration data for said programmable logic circuit (col.2, ll.41-50; col.2, ll.55-65; col.6, ll.10-24; col.11, ll.34-50);

reconfiguring a programmable logic circuit of a system under test (evolvable hardware) with a circuit design according to said configuration data for said test job (a method for evolving configuration bitstreams for programmable logic devices - col.1, ll.35-36) by way of said test sever (col.1, ll.33-36; col.2, ll.45-50; col.2, ll.55-65);

coupling said test vectors to said system under test (col.2, ll.45-47);

receiving an output comprising result vectors from said system under test (col.2, ll.48-50); and

comparing said result vectors from said system under test to expected result vectors (col.2, ll.50-54);

(26) A method of verifying a semiconductor design by way of a server, said method comprising the steps of:

coupling a plurality of client computers lo a job distribution sever, each said client computer storing a test job for testing the design of a programmable logic circuit, said test job having test vectors and configuration data for said programmable logic circuit (col.2, ll.41-50; col.2, ll.55-65; col.6, ll.10-24; col.11, ll.34-50);

reconfiguring a programmable logic circuit of a system under test (evolvable hardware) with a circuit design according to said configuration data for said test job (a method for evolving configuration bitstreams for programmable logic devices - col.1, ll.35-36) by way of said test sever (col.1, ll.33-36; col.2, ll.45-50; col.2, ll.55-65);

coupling said test vectors to said system under test (col.2, ll.45-47);

receiving an output comprising result vectors from said system under test (col.2, ll.48-50); and

comparing said result vectors from said system under test to expected result vectors (col.2, ll.50-54).

5. As to claims 2-5, 7-10, 12-15, 17-20, 22-25 and 27-30 Levi recites:

(2), (4), (18) The system/method, wherein said client device further has expected results (col.2, ll.50-54);

(3), (17) The system/method, wherein said client device generates said test vectors (col.6, ll.10-24);

(5) The system, wherein said test vectors and said expected results are generated by an external device (col.6, ll.16-24; col.10, ll.25-39);

(7), (23) The system of claim 6 wherein said server comprises a network interface (col.2, ll.55-65);

(8), (9), (14), (20), (24), (30) The system/method, wherein said server comprises a system under test interface (col.2, ll.45-50; col.2, ll.55-65);

(10), (19) The system/method further comprising another server coupled to said plurality of client devices by way of the network (col.11, ll.35-51);

(12), (13), (15), (22), (27), (28), (29) The system/method further comprising a plurality of servers coupled to said plurality of client devices (col.11, ll.35-51);

(25) The method of claim 21 wherein said step of comparing comprises comparing said result vectors from said system under test to expected result vectors at said client device (col.2, ll.50-54).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B. Levin whose telephone number is 571-272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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STACY A. WHITMORE
PRIMARY EXAMINER